ELECTRICAL AND MATERIAL PROPERTIES OF METAL SILICATE DIELECTRICS AND METAL GATE ELECTRODES FOR ADVANCED CMOS DEVICES

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This paper reports on the electrical and material properties of ultra-thin hafnium silicate films ($HfSi_xO_y$) and the properties of various metal gate electrodes for advanced CMOS devices. Excellent C-V and I-V characteristics have been obtained with $HfSi_xO_y$ films with an equivalent oxide thickness of 1.2 nm, indicating that this material is an excellent gate dielectric candidate for aggressively scaled CMOS devices. Good stability of $HfSi_xO_y$ with polysilicon gate electrodes was achieved up to 900 °C. Aluminum, on the other hand, was found to readily interact with $HfSi_xO_y$ resulting in a tri-layer gate dielectric. Various metal gates were evaluated on SiO_2. TaN was found to provide reasonable gate current and optimal NMOSFET workfunction values. Ta resulted in higher gate leakage and had inferior thermal stability. Other metals such as Hf, Zr and Ti were found to be very inadequate causing a reduction of the dielectric.

INTRODUCTION

To ensure continued downscaling of CMOS, new materials for the gate dielectric and gate electrode are needed to overcome the fundamental problems of gate leakage, and gate depletion. Major activities are currently on going to investigate new gate dielectrics and metal gates as replacements for the current SiO_2/polysilicon gate stacks. In the area of gate dielectrics, metal oxides, such as ZrO_2, Ta_2O_5 and Al_2O_3, offer high capacitance without suffering from excessive gate leakage. However, most of these metal oxides display instabilities with the underlying silicon and grow an undesirable SiO_2 layer. The presence of this layer can reduce the total gate capacitance and also limit the ultimate achievable thickness. Therefore, the use of a Si compatible dielectric that does not require an interface layer and is thermally stable on Si is very attractive in obtaining the performance benchmarks set by the SIA roadmap.

Metal silicates, such as $ZrSiO_4$ and $HfSiO_4$, are projected to be thermodynamically stable on Si since these materials are formed by intermixing SiO_2 with a transition metal to increase the dielectric constant. The basis for the stability of these silicates lies in their tetragonal crystal structure which is very similar to SiO_2 and where each Zr and Si atom is bonded to four O atoms [1]. Ternary phase diagram of the Zr, Si and O system, shown in Fig 1, indicates a stable tie line between silicates and Si.

The dielectric constant of this material is projected to lie between SiO_2 and ZrO_2 or HfO_2 and has ε~12-20. Based on these material properties, these films are excellent candidates for gate dielectric applications. In fact, recent results on $HfSiO_4$ films have indicated excellent interfacial and bulk properties with a Tox equivalent of 1.8 nm [2].

To achieve 50 nm CMOS, it is also imperative that polysilicon gate electrodes be replaced with metallic electrodes that have carrier concentrations > 10^{22} cm^{-3}. The search for metallic gate electrodes for 50nm CMOS and beyond faces many challenges since new gate electrodes must have compatible work functions, process compatibility with dielectric deposition and annealing, and thermal/chemical interface stability with dielectrics. To replace n^+ and p^+ poly-silicon and maintain scaled performance, it is necessary to identify pairs of metals with workfunctions that are respectively within 0.2 eV of the conduction and valence band edges of Si, i.e., ϕ_m for NMOS and PMOS gates must be near 4eV and 5eV, respectively. It should be noted that midgap work function metals (e.g., TiN and W) are inadequate for advanced devices due to a) threshold voltages that are too large for low-voltage operation and b) severely degraded short channel characteristics.

This paper will discuss the electrical and material properties of ultra-thin hafnium silicate films ($HfSi_xO_y$) and the properties of various metal gate electrodes for advanced CMOS devices.

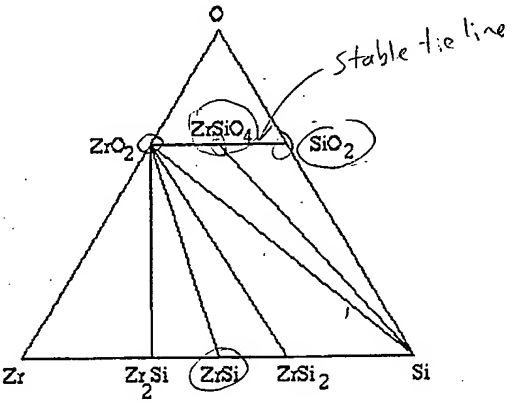


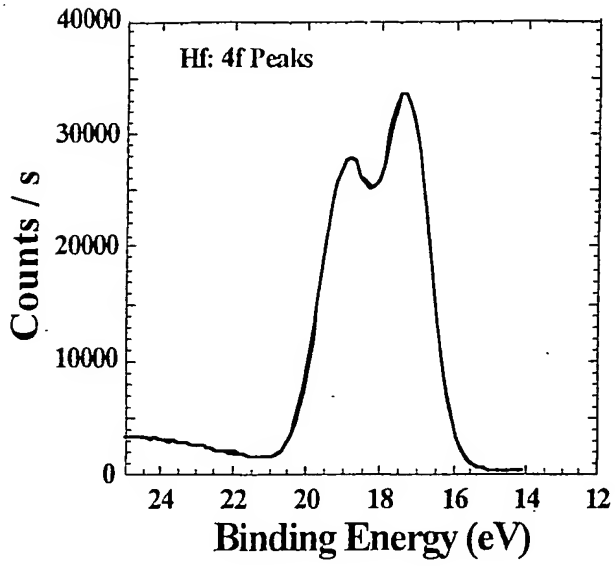
Fig 1. Ternary phase diagram for Zr-Si-O system.

EXPERIMENTAL

The $HfSi_xO_y$ dielectrics were deposited at room temperature using reactive sputtering of a $HfSi_2$ target in O_2 ambient. The process pressure was 10mTorr with equal partial pressure of O_2 and Ar. Several gate electrodes were used including Ta, TaN and N+ and P+ Polysilicon. This was followed by a post metallization anneal in N_2/H_2 at 400°C. Field oxide defined overlap capacitors on n and p-type substrates were fabricated. Metal definition was achieved via liftoff. Metals or metal nitrides gate electrodes were deposited using DC magnetron sputtering or reactive RF/DC magnetron sputtering. The metals were capped by W to avoid oxidation of the thin metal layers. Forming gas (10 $\%H_2$ / N_2) anneal at 400 °C for 30 minutes was performed.

Results: $HfSi_xO_y$

Material analysis of the $HfSi_xO_y$ films was performed using TEM and XPS to identify reaction layers and bonding in the silicate films. The XPS data is shown in Fig. 2. As shown, both Hf-4f and Si-2p peaks are detected. No peaks for Hf-Si bond are observed indicating the absence of Hf-Si bonds. The Si-2p Si-O peaks for various thicknesses shown in Fig. 2 are shifted from a pure SiO_2 film indicating that this film is a silicate.



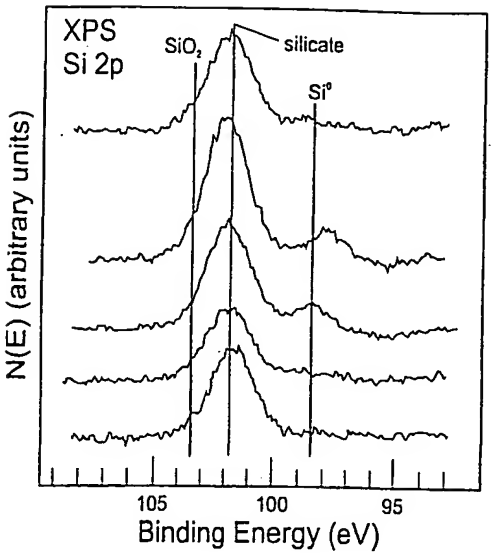


Fig 2. XPS analysis of $HfSi_xO_y$ films. (a) Hf-4f and (b) Si-2p.

Transmission electron microcopy with Al gates was performed to obtain the thickness of the film in an effort to obtain the dielectric constant of the film. As shown in Fig. 3, aluminum gates resulted in a tri-layer structure with a total thickness of 7.9 nm. The bottom layer in the TEM cross-section appeared to be SiO_2 rich. However, the physical thickness of this stack did not match the electrical CV results which indicated a oxide equivalent thickness (EOT) of 2.1 nm (Fig 4). This implied that the bottom layer next to the Si substrate contained a small amount of hafnium. However, it was not possible to determine whether the reaction layer near the Al gate was insulating or conducting which made it difficult to extract a dielectric constant with Al gates. Therefore, other electrodes such as Pt and polysilicon were evaluated both of which produced bi-layer structures as indicated via TEM.

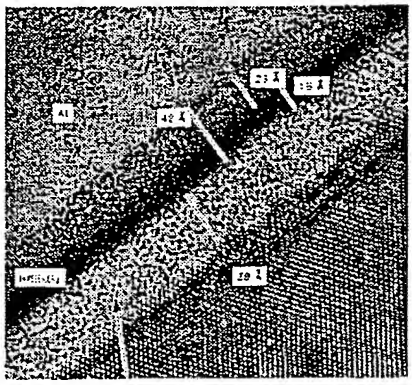


Fig. 3. Tranmission electron micrograph of $HfSi_xO_y$ film with Al gates.

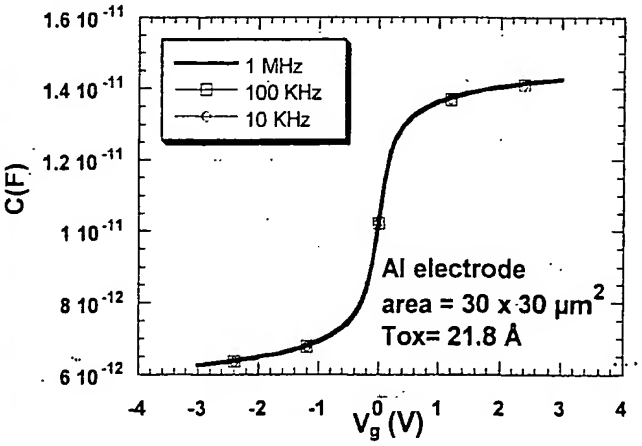


Fig. 4. MOS CV characteristics of Al gated $HfSi_xO_y$ films.

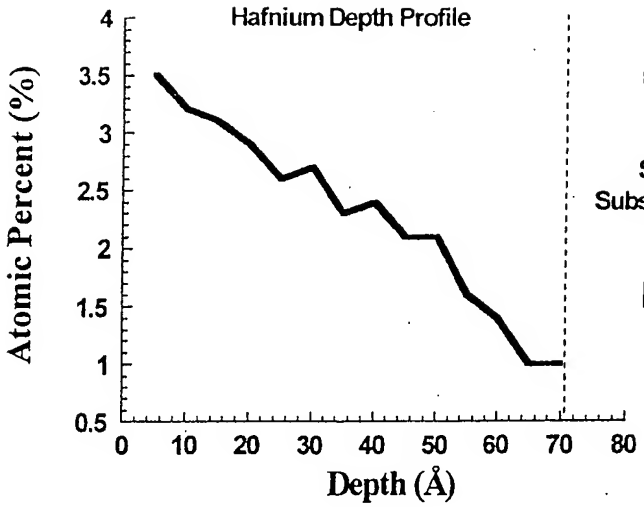


Fig. 5. Atomic percentage of Hf as a function of depth into the dielectric as determined by sputter XPS depth profiling.

In order to confirm and quantify the hafnium content in the interface layer, sputter XPS analysis on blanket $HfSi_xO_y$ films was performed. As shown in Fig 5, the hafnium content is graded through the dielectric and a small amount of hafnium was found near the Si interface. Although the atomic percentage of hafnium near the interface is low it is still resulting in an increase of the permittivity of the interfacial layer.

MOS capacitors were fabricated to evaluate the effect of an alternate and more stable gate electrode on the $HfSi_xO_y$ properties. To this end, N^+ polysilicon gates were deposited at 550 °C, followed by phosphorus disk diffusion for 30 minutes at 900 °C. TEM analysis of the above capacitors was performed and is shown in Fig. 6. A bilayer structure is observed with the layer near the Si substrate being more SiO_2-rich and the top layer being more metal rich layer. In addition, the gate dielectric stack appears to remain amorphous even after a 900 °C anneal. This thermal stability may be attributed to the low atomic content of Hf in these films.

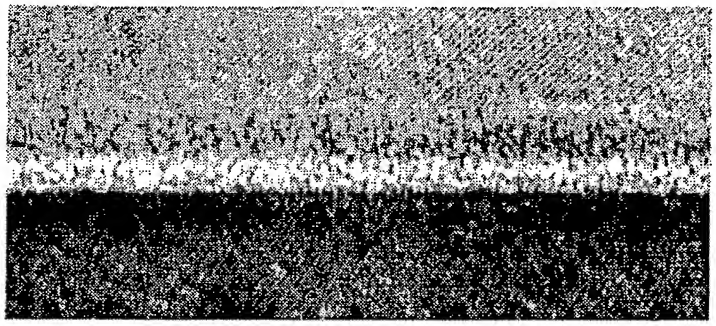


Fig. 6. Transmission electron spectroscopy of $HfSi_xO_y$ film with N^+ polysilicon gates.

MOS-CV characteristics were obtained on this film and are shown in Fig 7. The EOT of this dielectric stack using NCSU's CV model was ~2.6 nm and the flatband voltage was –0.936 V. This value of flatband voltage is close to ideal flatband voltage.

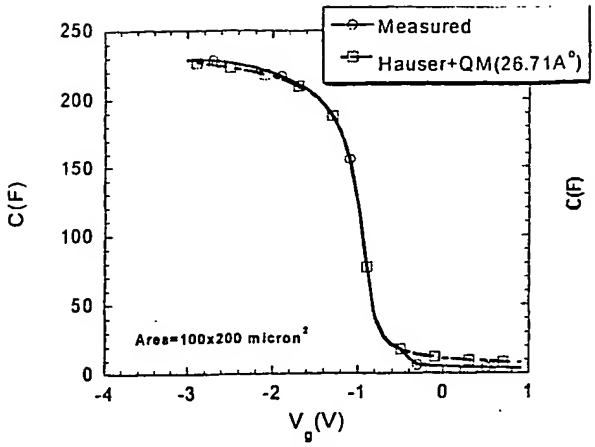


Fig. 7. MOS-CV of a $HfSi_xO_y$ film with N^+ polysilicon gates. The fit to NCSU's CV model is also shown.

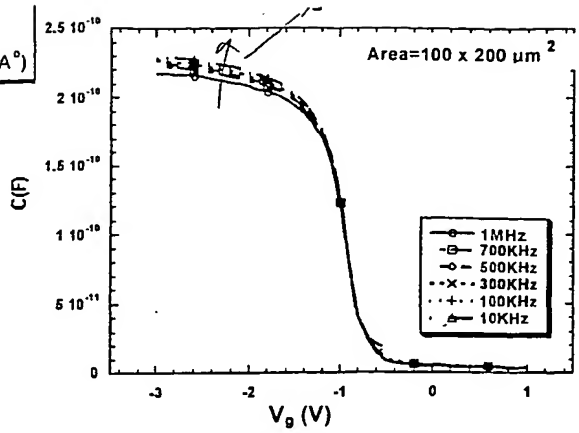


Fig. 8. Frequency dependence of a $HfSi_xO_y$ film. No significant frequency dependence is observed.

The physical thickness of this stack was 5.5 nm with bottom and top layer each being 2.5 nm. Taking the physical thickness into account reconfirms that the bottom layer is not pure SiO_2. The effective dielectric constant of this stack ranges from 7.5 to 8.5 and can be considered as a graded high-K dielectric.

Measurements were also taken at 10, 100, 300, 500, and 700 kHz and 1 MHz. It can be seen from Fig. 8 that there is no significant frequency dependence of the CV characteristics of $HfSi_xO_y$. Hysteresis measurements were also performed (not shown) and indicated no detectable change in the CV characteristics.

Along with capacitance measurements, gate current is another very significant metric for high-K dielectric evaluation. Although, the films in this work are considerably thicker than 1nm, they can still provide useful information on the conduction properties of these films. The gate current through N^+/p substrates is shown in Fig. 9. As evident, the leakage current through this material is quite reasonable for an EOT of 2.6 nm.

Results: Metal Gates

This section discusses metal gate stability on SiO_2. As discussed earlier, metal gates are needed to achieve desired performance benchmarks for 50 nm CMOS devices. Polysilicon does not have high dopant activation at the gate/dielectric interface. Furthermore, polysilicon may be incompatible with high-K dielectric candidates due to formation of a SiO_2 layer between the gate/dielectric interface. In addition, sheet resistance and boron diffusion from P^+ polysilicon are also issues for sub-100nm gate lengths.

In this work, metal electrodes were evaluated on SiO_2. The evaluation of metal electrodes interaction with SiO_2 can provide information on predicting the stability and workfunction of various metals on high-K dielectrics. Both metals and metal nitrides were investigated on SiO_2. The motivation behind investigating a metal and its corresponding metal nitride was the increase in workfunction expected upon the introduction of nitrogen. Initial results of workfunction evaluation of various gate electrodes on SiO_2 are shown in Fig. 10. The flatband voltages indicated that the work

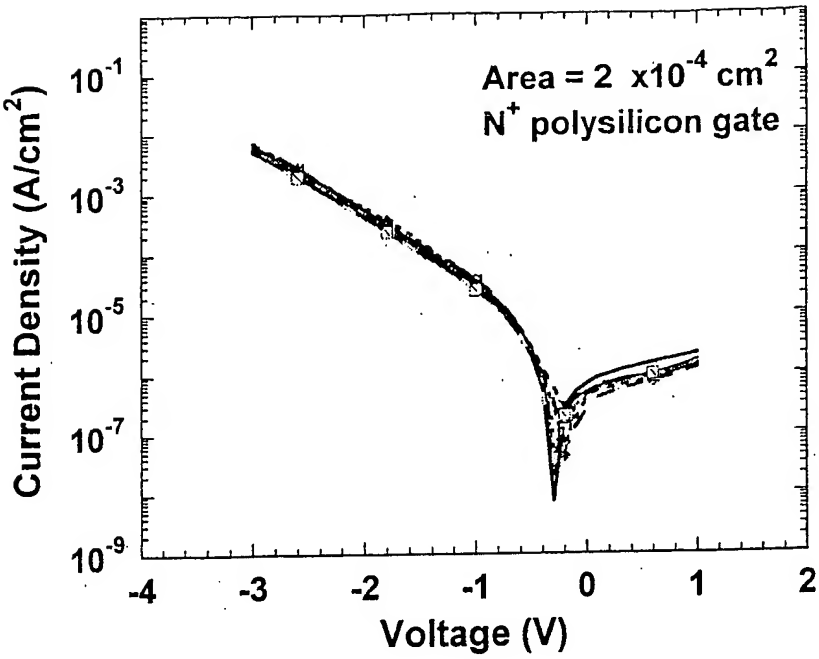


Fig. 9. Gate current density for $HfSi_xO_y$ film with N^+ gate and an EOT of 2.6 nm.

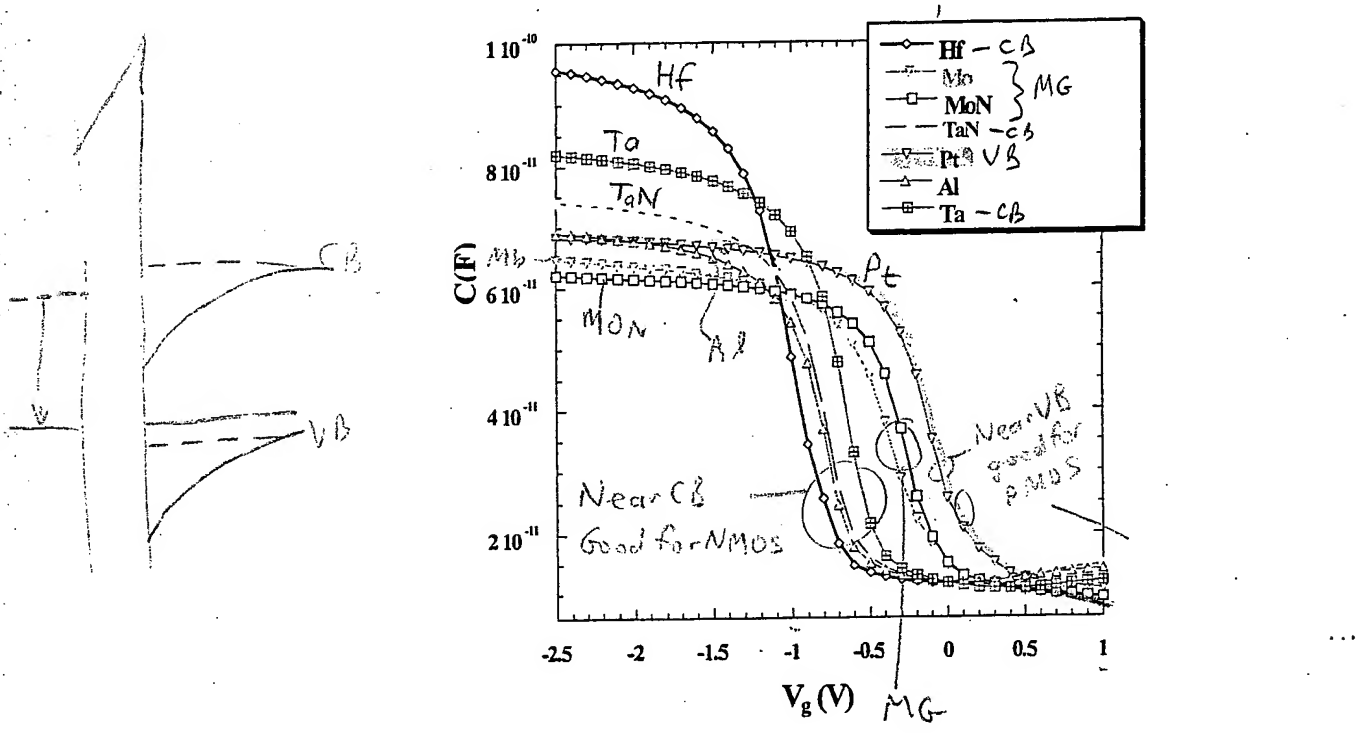


Fig. 10. Flatband and capacitance for various metal electrodes.

function of Ta, TaN, Ti, Hf, Zr were all near the conduction band of Si, and Pt was near the valence band and HfN, Mo and MoN were near the midgap. It should be noted that contrary to expectation, no workfunction difference was observed between Ta and TaN films even though the nitrogen incorporation in TaN films was found to be around 40% obtained via RBS measurements. Tantalum gates on SiO_2 displayed a small degree of instability and had higher leakage compared to TaN and other metals. This was believed to be occurring either due to a) formation of Ta_2O_5 or b) diffusion of Ta in SiO_2 [3]. The thermal reactions at the metal-dielectric interface were also monitored before and after anneal. Hafnium gate electrodes were found to be highly unstable on SiO_2 as anneal temperature increased. As shown in Fig. 11, the anneal treatments decreased the oxide thickness and increased the leakage current. Transmission electron microscopy, RBS and XPS indicated that Hf consumes the gate dielectric with excess oxygen diffusing to the top of the metal film resulting in the incorporation of oxygen finally leading to the formation of HfO_2 which brings the reaction to completion. This reaction is strongly temperature dependent and can be predicted by thermodynamics. Similar instabilities can be predicted for Ti, TiN and Zr electrodes [4].

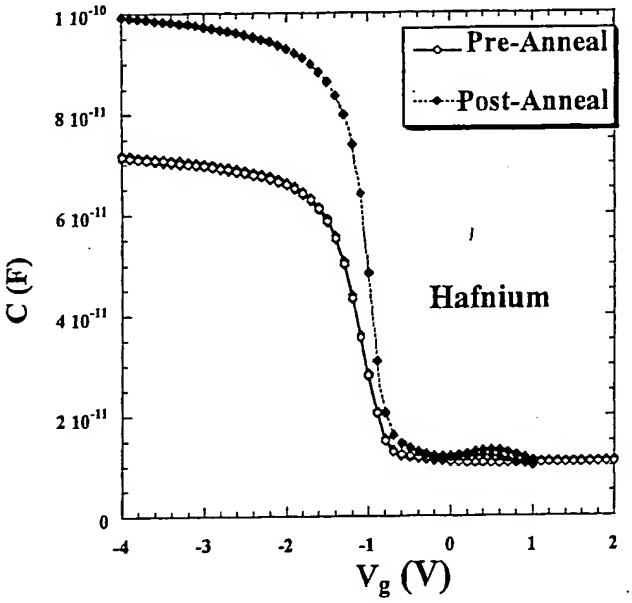


Fig. 11. Change in oxide capacitance with a hafnium gate electrode after a 400 °C PMA.

DISCUSSION

There are some general trends in anticipated properties that can be drawn from the extensive studies of metal-Silicon contacts, as well as basic bonding chemistry trends of bulk properties as a function of electronegativity. These include the following; i) in general, work functions with respect to vacuum increase, as the electronegativity of the metal, metal compound or metal silicide increases; ii) since Si has a higher electronegativity than many transition metals, and an electronegativity that is less than or comparable to many noble metals, the metal silicide work functions are generally in the lower half of the band gap of Si; iii) the work functions of metal oxides and nitrides are larger than those of the metals: e.g., the work functions of transition metal nitrides such as TiN_X and WN_X are near mid-gap, whereas as the work functions of noble metal oxides

such as iridium oxide are closer to the valence band edge and iv) work functions of silicides are anticipated to span almost the entire Si band gap, but in general be more suitable for PMOS than NMOS devices. It is important to note that interfacial dipoles will contribute to valence band offset energies at both Si-dielectric and metal-dielectric interfaces, and that the potential steps associated with the dipoles can be additive, or partially-compensating. Therefore each candidate metal must be evaluated with respect to different emerging high-K materials with different results possible. There are many choices available for the optimum workfunction, however stability will depend on electronegativity and metals with $\chi < 1.5$ tend to react with SiO_2. Typical examples of this reaction includes Zr,Ti, Hf, V, and Nb. This means that many of the transition metals with vacuum work functions that are candidates for NMOS applications will be reactive on SiO_2, and perhaps Si_3N_4 surfaces. Their reactivity may differ appreciably on different high K oxides, according to their average electronegativity, or equivalently the fraction of ionic bonding. In general, if silicide reactions are possible between metals and the underlying gate dielectric as in $ZrSiO_4$ or TiO_2-SiO_2 alloys, these will tend to drive the effective metal work functions toward midgap. These evaluations of metals on SiO_2 can provide useful predictions of reactivity on high-K dielectrics.

CONCLUSIONS

In summary, excellent C-V and I-V characteristics have been obtained with $HfSi_xO_y$ films with an equivalent oxide thickness of 1.2 nm, indicating that this material is an excellent gate dielectric candidate for aggressively scaled CMOS devices. These were corroborated with TEM and XPS results which indicated the formation of a bilayer, amorphous sub-silicate film with a Hf-content of 6-7 %. Good stability of $HfSi_xO_y$ with polysilicon gate electrodes was achieved up to 900 °C. Aluminum, on the other hand, was found to readily interact with $HfSi_xO_y$ resulting in a tri-layer gate dielectric. Various metal gates were evaluated on SiO_2. TaN was found to provide reasonable gate current and optimal NMOSFET workfunction values. Ta resulted in higher gate leakage and had inferior thermal stability. Other metals such as Hf, Zr and Ti were found to be very inadequate causing a reduction of the dielectric.

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